University of Jordan
School of Engineering
Electrical Engineering Department

EE 204
Electrical Engineering Lab

EXPERIMENT 2
DC CIRCUITS

Prepared by: Prof. Mohammed Hawa

EXPERIMENT 2
RESISTORS AND DC CIRCUITS

OBJECTIVE

When you have completed this exercise, you will know about the different resistor types, and learn the resistor color code. You will also test different DC circuit analysis techniques, including parallel/series combinations, voltage/current division, and nodal/mesh analysis.

DISCUSSION

Nodal and Mesh Analysis

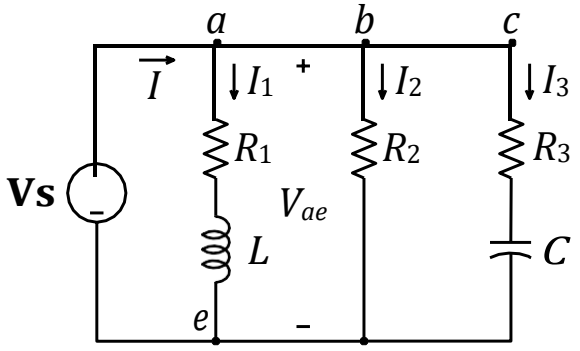
Electric circuits may be analyzed using a node voltage technique or a mesh current technique. In nodal analysis, all circuit nodes are first identified, a node being a point where various branches combine. A reference node, usually ground, is included. Kirchhoff's Current Law (KCL) is then applied to each node. KCL states that the sum of currents entering a node must equal the sum of the currents exiting that node. Consequently a set of simultaneous equations are created with an unknown voltage for each node with the exception of the reference. Once the node voltages are determined, various branch currents and component voltages may be derived.

In mesh analysis, a minimum number of small loops are identified in the circuit. The loop currents are referred to as mesh currents as each current interlocks or meshes with the surrounding loop currents. Kirchhoff's Voltage Law (KVL) is then applied to each loop. KVL states that the sum of voltages around a loop must equal zero. Hence, a set of simultaneous equations is created, which can be solved for unknown mesh currents. Once the mesh currents are determined, various branch currents and component voltages may be derived.

PROCEDURE A – CAPACITORS AND INDUCTORS IN DC CIRCUITS

In this PROCEDURE section, you will investigate the behavior of capacitors and inductors within DC circuits.

1. Construct the circuit shown below. Assume that R_1 = 1700Ω, R_2 = 1200Ω, R_3 = 1000Ω, L = 100mH, and C = 0.1μF.



2. Set the DC supply output voltage controls to minimum then connect it to the circuit. Switch the DC supply ON, and set its voltage Vs to 9 Volts. Verify this voltage using a voltmeter.

3. Using theoretical analysis determine the expected currents I_1, I_2, I_3 and I along with the voltage V_{ae}. Record these values in Table 5. What is the current divider equation for the current in resistor R_1?

. . . . . .

4. Use the DMM to measure the currents I_1, I_2, I_3 and I along with the voltage V_{ae}. Record these values in Table 1.

Table 1

	I_1 (mA)	I_2 (mA)	I_3 (mA)	$I_1+I_2+I_3$	I (mA)	V_{ae} (V)
Theory						
Measured						

5. What happens to inductors in DC circuits?

. . . . . .

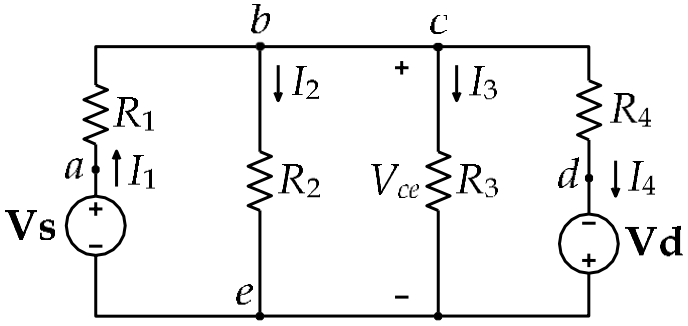
6. What happens to capacitors in DC circuits?

. . . . . .

PROCEDURE B – NODAL AND MESH ANALYSIS

In this PROCEDURE section, you will apply nodal and mesh analysis to multi-source DC circuits.

1. Construct the dual-supply circuit shown below. Assume that R_1 = 1200Ω, R_2 = 2200Ω, R_3 = 1000Ω, and R_4 = 1700Ω.



2. Set the DC supplies output voltage controls to minimum then connect them to the circuit. Switch both DC supplies ON, and set their voltages to Vs = 9 Volts and Vd = 14 Volts. Verify these voltages using a voltmeter.

3. Use **nodal** analysis to calculate the theoretical values of the voltages V_{ae}, V_{be}, V_{ce} and V_{de}. Record these values in Table 2. What was the nodal equation you wrote at node *b*?

. . . . . .

4. Use the DMM to measure the voltages V_{ae}, V_{be}, V_{ce} and V_{de}. Record these values in Table 2.

Table 2

	V_{ae} (V)	**V_{be} (V)**	**V_{ce} (V)**	**V_{de} (V)**
Theory				
Measured				
Deviation (%)				

5. Now use **mesh** analysis to calculate the theoretical values of the currents I_1, I_2, I_3 and I_4. Record these values in Table 3. What was the mesh equation you wrote for the *left* mesh?

. . . . . .

6. Use the DMM to measure the currents I_1, I_2, I_3 and I_4. Record these values in Table 3.

Table 3

	I_1 (mA)	**I_2 (mA)**	**I_3 (mA)**	**I_4 (mA)**
Theory				
Measured				
Deviation (%)				

**** End ****